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DATA SHEET

SAA1101
Universal sync generator (USG)

Product specification
File under Integrated Circuits, IC02

January 1990

Philips
Semiconductors

PHILIPS

Universal sync generator (USG) SAA1101

FEATURES

- Programmable to seven standards
- Additional outputs to simplify signal processing
- Can be synchronized to an external sync. signal
- Option to select the 524/624 line mode instead of the 525/625 line mode
- Lock from subcarrier to line frequency

GENERAL DESCRIPTION

The SAA1101 is a Universal Sync Generator (USG) and is designed for application in video sources such as cameras, film scanners, video generators and associated apparatus. The circuit can be considered as a successor to the SAA1043 sync generator and the SAA1044 subcarrier coupling IC.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage range (pin 28)	4.5	5.5	V
I_{DD}	quiescent supply current	–	10	µA
f_{OSC}	clock oscillator frequency	–	24	MHz

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA1101P	28	DIL	plastic	SOT117 (1)
SAA1101T	28	SO28	plastic	SOT136A (2)

Notes

1. SOT117-1; 1996 December 02.
2. SOT136-1; 1996 December 02.

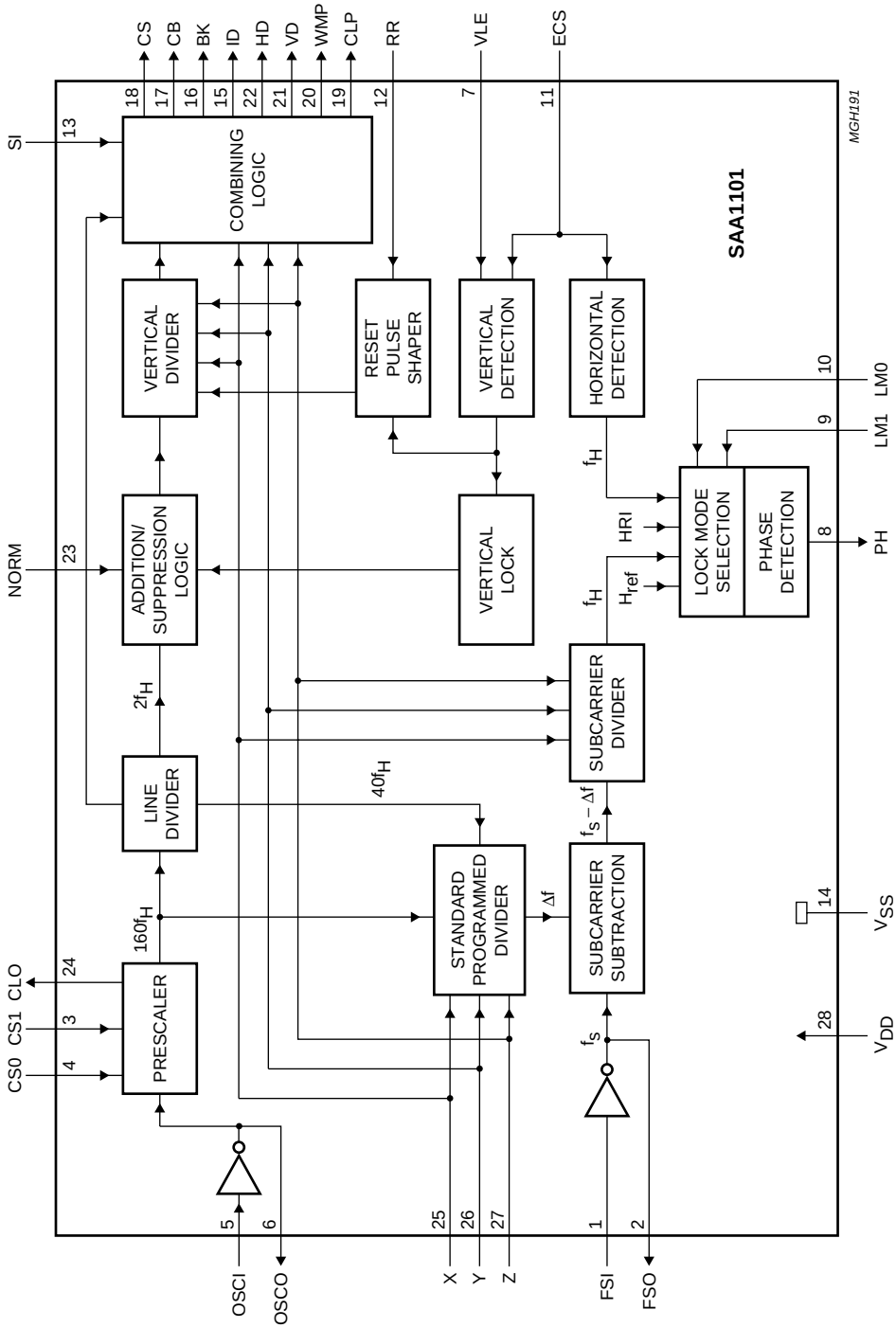


Fig.1 Block diagram.

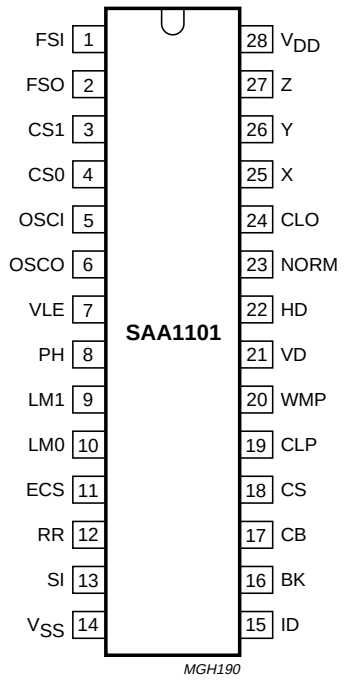


Fig.2 Pinning configuration; SOT117.

FUNCTIONAL DESCRIPTION

Generation of pulses

Generation of standard pulses such as sync, blanking and burst for TV systems: PAL B/G, PALN, PALM, SECAM and NTSC. In addition a number of non-standard pulses have been supplied to simplify signal processing. These signals include - horizontal drive, vertical drive, clamp pulse, identification etc. It is possible to select the 524/624 line mode instead of the 525/625 line mode for all the above TV systems for applications such as robotics, games and computers.

PINNING

SYMBOL	PIN	DESCRIPTION
FSI	1	subcarrier oscillator input, where f_{max} = 5 MHz
FSO	2	subcarrier oscillator output
CS1	3	clock frequency selection - CMOS input
CS0	4	clock frequency selection - CMOS input
OSCI	5	clock oscillator input, where f_{max} = 24 MHz
OSCO	6	clock oscillator output
VLE	7	vertical in-lock enable - CMOS input
PH	8	phase detector output - 3-state output
LM1	9	lock mode selection - CMOS input
LM0	10	lock mode selection - CMOS input
ECS	11	external composite sync. signal - CMOS Schmitt-trigger input
RR	12	frame reset - CMOS Schmitt-trigger input
SI	13	set identification, used to set the correct field sequence in PAL-mode. The correction (inversion of fH2) is done at the left-hand slope of the SI-pulse. Minimum pulse width is 800 ns. CMOS Schmitt-trigger input.
V_{SS}	14	ground
ID	15	identification - push-pull output
BK	16	burst key (PAL/NTSC), chroma-blanking (SECAM) - push-pull output
CB	17	composite blanking - push-pull output
CS	18	composite sync. - push-pull output
CLP	19	clamp pulse - push-pull output
WMP	20	white measurement pulse-3-state output
VD	21	vertical drive pulse - push-pull output
HD	22	horizontal drive pulse - push-pull output
NORM	23	used with X, Y and Z to select TV system; NORM = 0, 625/525 line mode (standard); NORM = 1, 624/524 line mode - CMOS input
CLO	24	clock output - push-pull output
X	25	TV system selection input - CMOS input
Y	26	TV system selection input - CMOS input
Z	27	TV system selection input - CMOS input
V_{DD}	28	voltage supply

Lock modes

The USG offers four lock modes:

- Lock from the subcarrier
- Slow sync. lock, external H_{ref}
- Slow sync. lock, internal H_{ref}
- Fast sync. lock, internal H_{ref}

LOCK FROM SUBCARRIER

Lock from subcarrier to the line frequency for the above mentioned TV systems is given below; the horizontal frequency (f_H) = 15.625 kHz for 625 line systems and 15.734264 kHz for 525 line systems.

SECAM (1 and 2)	$282f_H$
PALN	$229.2516f_H$
NTSC (1 and 2)	$227.5f_H$
PALM	$227.25f_H$
PAL B/G	$283.7516f_H$

These relationships are obtained by the use of a phase locked loop and the internal programmed divider chain, see Fig.3(a).

LOCK TO AN EXTERNAL SIGNAL SOURCE

The following methods can be used to lock to an external signal source:

1. Sync. lock slow; the line frequency is locked to an external signal. The line and frame information are extracted from the external sync. signal and used separately in the lock system. The line information is used in a phase-locked loop where external and internal line frequencies are compared by the same phase detector as is used for the subcarrier lock. The external frame information is compared with the internal frame in a slow lock system; mismatch of internal and external frames will result in the addition or suppression of one line depending on the direction of the fault. The maximum lock time for frame lock is 6.25 s, see Fig.3(b).
2. Sync. lock fast. A fast lock of frames is possible with a frame reset which is extracted out of the incoming external sync. signal, see Fig.3(c).
3. Sync. lock with external reference. Lock of an external sync. signal to the line frequency with an external line reference to make possible a shifted lock. The subcarrier input is, in this case, used as an external input for the horizontal reference, see Fig.3(d).

SELECTION OF LOCK MODE

Lock mode is selected using the inputs LM0 and LM1 as illustrated in the Table below.

LM0	LM1	SELECTION
0	0	lock to subcarrier
0	1	slow sync. lock external H_{ref}
1	0	slow sync. lock internal H_{ref}
1	1	fast sync. lock internal H_{ref}

The different lock modes are illustrated by the following figures:

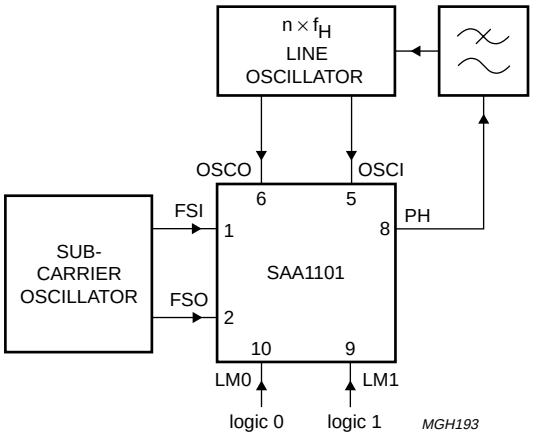


Fig.3 (a) Lock to subcarrier.

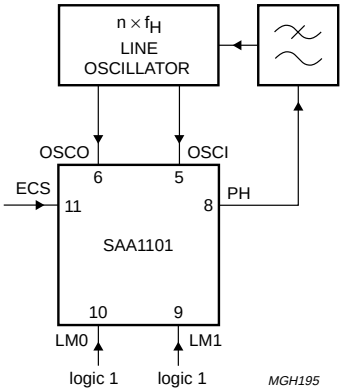


Fig.3 (c) Fast sync lock, internal H_{ref}

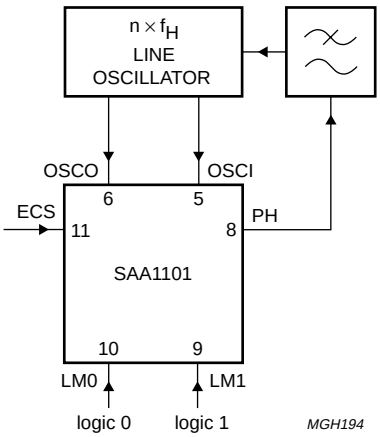


Fig.3 (b) Slow sync lock, internal H_{ref}

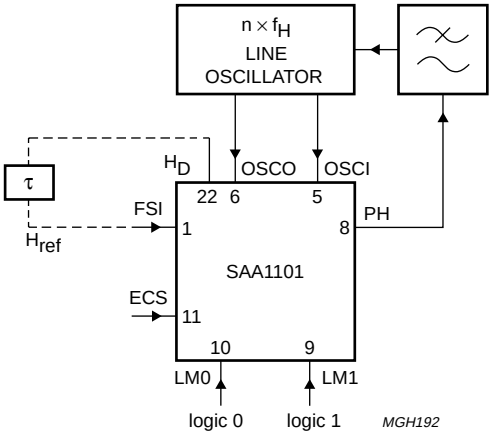


Fig.3 (d) Slow sync lock, external H_{ref}

LOCK WITH HORIZONTAL AND VERTICAL SIGNALS

(slow lock modes only)

It is possible to use horizontal and vertical signals instead of composite sync signals. The connections in this situation are: the external horizontal signal is connected to the ECS input (pin 11) and the vertical signal to the RR input (pin 12). The HIGH time of the horizontal pulse must be less than 14.4 μs, otherwise it will be detected as being a vertical pulse and will corrupt the vertical slow lock system.

Selection of Clock Frequency

The clock frequency is selected using the CS0 and CS1 inputs as illustrated below.

CS0	CS1	FREQUENCY	625 LINES	525 LINES	UNITS
0	0	$160f_H$	2.5	2.517482	MHz
0	1	$160f_H$	5	5.034964	MHz
1	0	$960f_H$	15	15.104893	MHz
1	1	$1440f_H$	22.5	22.657340	MHz

Where the horizontal frequency, f_H = 15.625 kHz for 625 lines and 15.734264 kHz for 525 lines.

Oscillators

The subcarrier oscillator has FSI as its input and FSO as its output. It is always used as a crystal oscillator with a series resonance crystal with parallel load capacitor. The maximum frequency, f_{max} = 5 MHz and the load capacitor, $C_L = 10 < C_L < 35$ pF.

The clock oscillator has OSCI as its input and OSCO as its output. It can be used with an LC oscillator or a series resonance crystal with parallel load capacitor (Fig.4). The maximum frequency, f_{max} = 24 MHz and the load capacitor, $C_L = 10 < C_L < 35$ pF.

Selection of 625/525 (standard; interlaced mode) or 624/524 lines (non-interlaced mode)

Selection is achieved using the NORM input. When NORM = 0, 625/525 (standard) lines are selected; when NORM = 1, 624/524 line are selected.

Output Dimensions

All push-pull outputs: standard output 2 mA.

White measurement pulse, WMP: 3-state output 2 mA.

Phase detector, PH: 3-state output 2 mA.

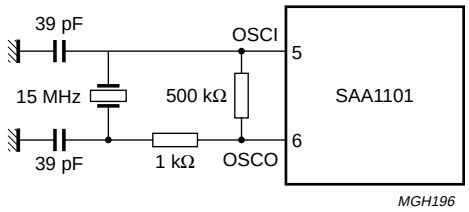


Fig.4 Crystal oscillator circuit.

Selection of TV System

Selection of the required TV system is achieved by the X, Y and Z inputs as illustrated by the following Table.

SYSTEM	X	Y	Z
SECAM1	0	0	0
PALN	0	0	1
NTSC1	0	1	0
PALM	0	1	1
SECAM2	1	0	0 (with identifier)
PAL B/G	1	0	1
NTSC2	1	1	0 (short blanking)

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	–0.5	+7	V
V_I	input voltage	–0.5	$V_{DD} + 0.5$ (1)	V
I_I	maximum input current	–	±10	mA
I_O	maximum output current	–	±10	mA
I_{DD}	maximum supply current in V_{DD}	–	25	mA
P_{tot}	maximum power dissipation	–	400	mW
T_{stg}	storage temperature range	–55	+150	°C

Note

1. Input voltage should not exceed 7 V.

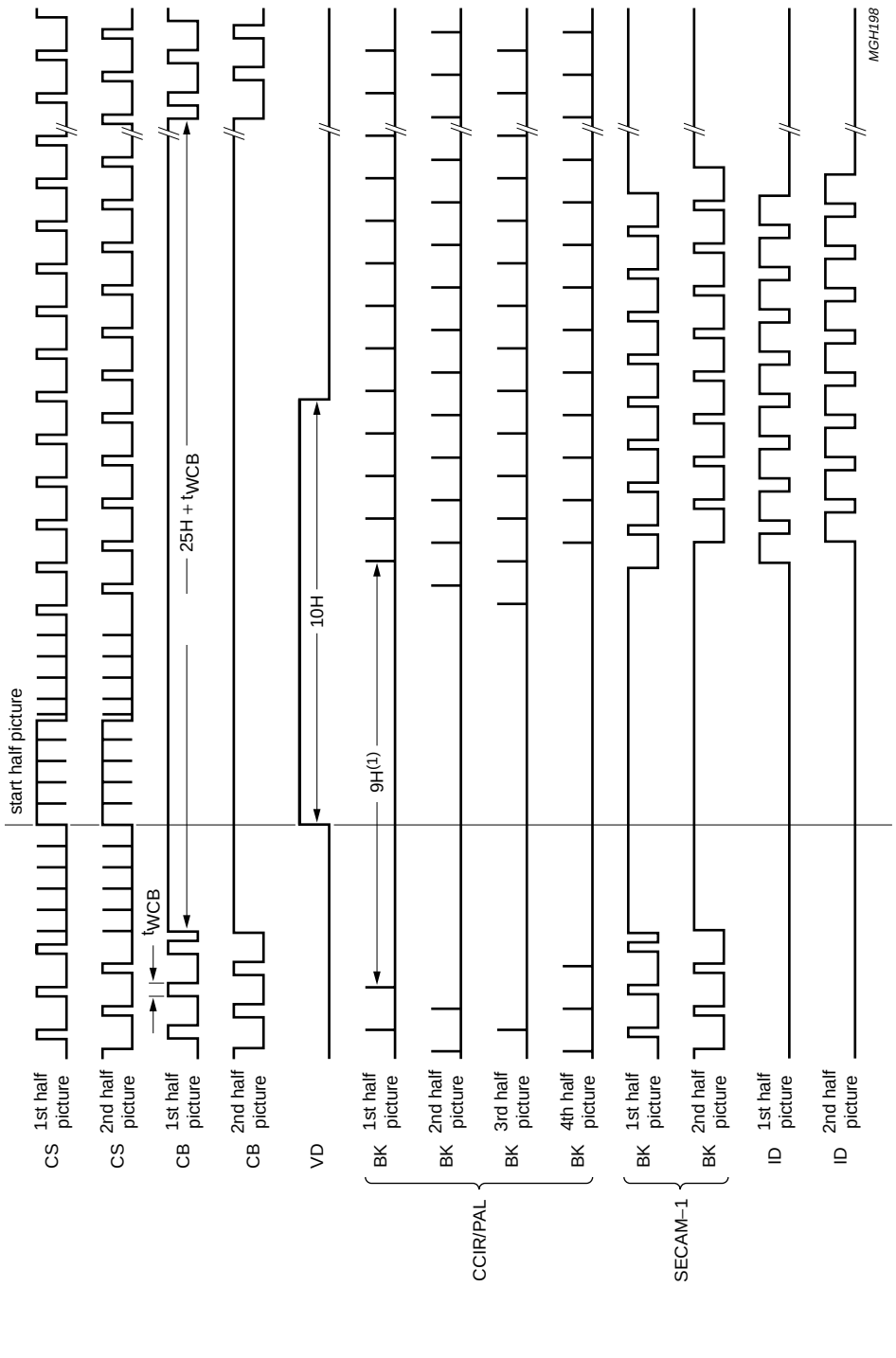
CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; T_{amb} = –25 to +70 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage		4.5	–	5.5	V
I_{DD}	supply current (quiescent)	T_{amb} = 25 °C	–	–	10	μA
Inputs						
$\pm I_I$	input leakage current	T_{amb} = 25 °C	–	–	100	nA
CMOS COMPATIBLE; X, Y, Z, NORM, CS0, CS1, LM0, LM1 AND VLE						
V_{IH}	input voltage HIGH		$0.7V_{DD}$	–	–	V
V_{IL}	input voltage LOW		–	–	$0.3V_{DD}$	V
SCHMITT TRIGGER INPUTS; ECS, RR AND SI						
V_{T+}	positive-going threshold		–	2.5	4	V
V_{T-}	negative-going threshold		1	1.5	–	V
V_H	hysteresis		0.4	1	–	V
OSCILLATOR INPUTS; OSCI AND FSI						
V_{IH}	input voltage HIGH		$0.7V_{DD}$	–	–	V
V_{IL}	input voltage LOW		–	–	$0.3V_{DD}$	V
Outputs						
PUSH-PULL OUTPUTS; CB, CS, BK, ID, HD, VD, CLP AND CLO						
V_{OH}	output voltage HIGH	$-I_O$ = 2 mA; V_{DD} = 5 V	4.5	–	–	V
V_{OL}	output voltage LOW	I_O = 2 mA; V_{DD} = 5 V	–	–	0.5	V
OSCILLATOR OUTPUTS; OSCO AND FSO						
V_{OH}	output voltage HIGH	$-I_O$ = 0.75 mA; V_{DD} = 5 V	4.5	–	–	V
V_{OL}	output voltage LOW	I_O = 0.75 mA; V_{DD} = 5 V	–	–	0.5	V
3-STATE OUTPUTS; WMP AND PH						
V_{OH}	output voltage HIGH	$-I_O$ = 2 mA; V_{DD} = 5V	4.5	–	–	V
V_{OL}	output voltage LOW	I_O = 2 mA; V_{DD} = 5V	–	–	0.5	V
$\pm I_{OZ}$	OFF-state current	T_{amb} = 25 °C	–	–	50	nA

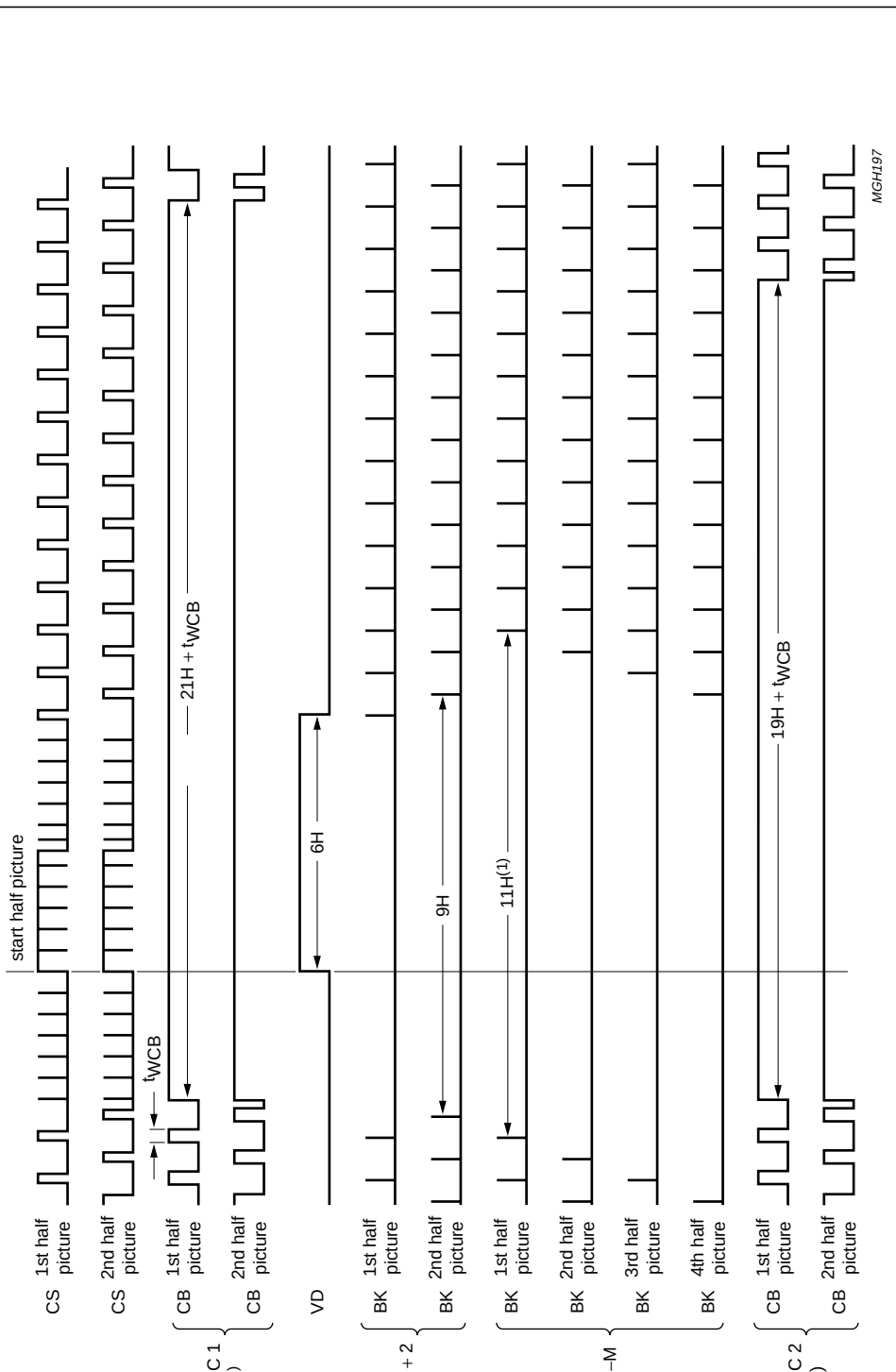
OUTPUT WAVEFORMS

The output waveforms for the different modes of operation are illustrated by Figs 5 and 6.



(1) H = 1 horizontal scan.

Fig.5 Typical output waveforms for PAL/CCIR and SECAM. In the 624-line mode the output waveforms are identical to the first half picture of PAL/CCIR and are not interlaced.



(1) H = 1 horizontal scan.
(2) NTSC mode reset; the fourth half picture is identical to the second half picture for NTSC.

Fig.6 Typical output waveforms for NTSC and PAL-M. In the 524-line mode the output waveforms are identical to the first half picture of NTSC and are not interlaced.

WAVEFORM TIMING

The waveform timing depends on the frequency of the oscillator input (f_{OSCI}). This is illustrated in the table below as the number (N) of oscillations at OSCI. The timings are derived from $N \times t_{OSCI} \pm 100$ ns.

One horizontal scan (H) = $320 \times t_{OSCI} = 1/f_H$.

Where t_{OSCI} = 200 ns for PAL/SECAM and 198.6 ns for NTSC/PAL-M

SYMBOL	PARAMETER	PAL	NTSC	PAL-M	SECAM	UNIT	N
Composite sync (CS)							
t_{WSC1}	horizontal sync pulse width	4.8	4.77	4.77	4.8	µs	24
t_{WSC2}	equalizing pulse width	2.4	2.38	2.38	2.4	µs	12
t_{WSC3}	serration pulse width	4.8	4.77	4.77	4.8	µs	24
–	duration of pre-equalizing pulses	2.5	3	3	2.5	H	–
–	duration of post-equalizing pulses	2.5	3	3	2.5	H	–
–	duration of serration pulses	2.5	3	3.5	2.5	H	–
Composite blanking (CB)							
HORIZONTAL BLANKING PULSE WIDTH							
t_{WCB}	PAL/SECAM/PAL-M	12	–	11.12	12	µs	60
t_{WCB}	NTSC1	–	11.12	–	–	µs	56
t_{WCB}	NTSC2	–	10.53 (note1)	–	–	µs	53
FRONT PORCH							
t_{PCBCS}	front porch	1.6	1.59	1.59	1.6	µs	8
DURATION OF VERTICAL BLANKING							
–	PAL/SECAM/PAL-M	$25H + t_{WCB}$	–	$21H + t_{WCB}$	$25H + t_{WCB}$	–	–
–	NTSC1	–	$21H + t_{WCB}$	–	–	–	–
–	NTSC2	–	$19H + t_{WCB}$	–	–	–	–
Burst key (BK) (not SECAM)							
t_{WBK}	burst key pulse width	2.4	2.38	2.38	–	µs	12
t_{PCSBK}	CS to burst key delay	5.6	5.56	5.76	–	µs	28
–	burst suppression	9	9	11	–	H	–
POSITION OF BURST SUPPRESSION							
–	first half picture	H623 to H6	H523 to H6	H523 to H8	–	–	–
–	second half picture	H310 to H318	H261 to H269	H260 to H270	–	–	–
–	third half picture	H622 to H5	H523 to H6	H522 to H7	–	–	–
–	fourth half picture	H311 to H319	H261 to H269	H259 to H269	–	–	–

SYMBOL	PARAMETER	PAL	NTSC	PAL-M	SECAM	UNIT	N
Burst key (BK) (SECAM)							
t_{WBK}	chroma pulse width	–	–	–	7.2	µs	36
t_{PBKCS}	CS to chroma delay	–	–	–	1.6	µs	8
DURATION OF VERTICAL BLANKING							
–	SECAM1	–	–	–	note 2	–	–
–	SECAM2	–	–	–	note 3	–	–
Clamp pulse (CLP)							
t_{WCLP}	clamp pulse width	2.4	2.38	2.38	2.4	µs	12
t_{PCSCLP}	CS to CLP delay	1.6	1.59	1.59	1.6	µs	8
Horizontal drive (HD)							
t_{WHD}	pulse width	7.2	7.15	7.15	7.2	µs	36
t_{PHDCS}	CS to HD delay	0.8	0.79	0.79	0.8	µs	4
–	repetition period	64	63.56	63.56	64	µs	–
Vertical drive (VD)							
–	VD duration	10	6	6	10	H	–
t_{PVDCS}	CS to VD delay	1.6	1.59	1.59	1.6	µs	8
White measurement pulse (WMP)							
–	pulse width	2.4	2.38	2.38	2.4	µs	12
–	CS to WMP delay	34.4	34.16	34.16	34.4	µs	172
–	duration of WMP	10	9	9	10	H	–
POSITION OF WMP							
–	first half picture	H163 to H173	H134 to H143	H134 to H143	H163 to H173	–	–
–	second half picture	H475 to H485	H396 to H405	H396 to H405	H475 to H485	–	–
Identification (ID)							
t_{WID}	pulse width	12	11.12	11.12	12	µs	60
t_{PIDCS}	CS to ID delay	1.6	1.59	1.59	1.6	µs	8
POSITION OF ID							
–	first half picture	H7 to H15	H8 to H22	H8 to H22	H7 to H15	–	–
–	second half picture	H320 to H328	H271 to H285	H271 to H285	H320 to H328	–	–

Notes to the characteristics

1. Horizontal blanking pulse width for NTSC2 can be 11.12 µs maximum
2. SECAM1, first half picture: 25H + t_{WBK} except H320 to H328. Second half picture: 24.5H + t_{WBK} except H7 to H15.
3. SECAM2, first half picture: 25H + t_{WBK}. Second half picture: 24.5H + t_{WBK}.

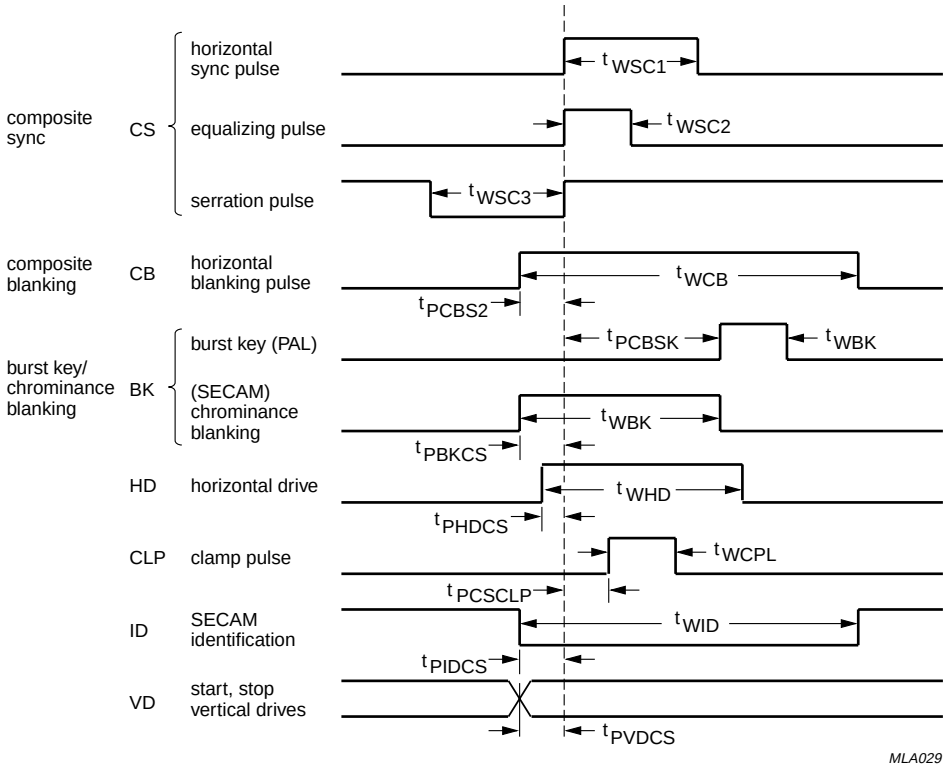
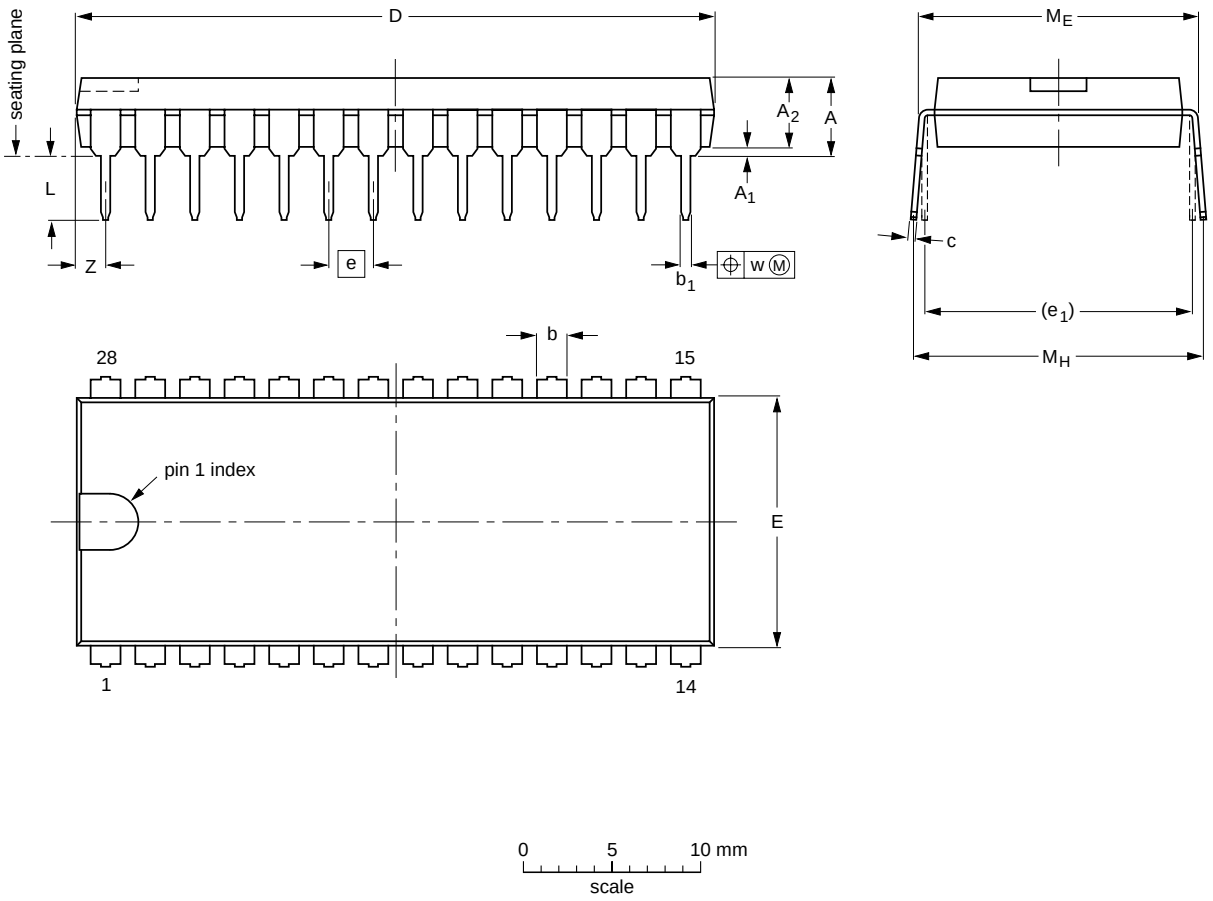


Fig.7 Waveform timing.

PACKAGE OUTLINES

DIP28: plastic dual in-line package; 28 leads (600 mil) **SOT117-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

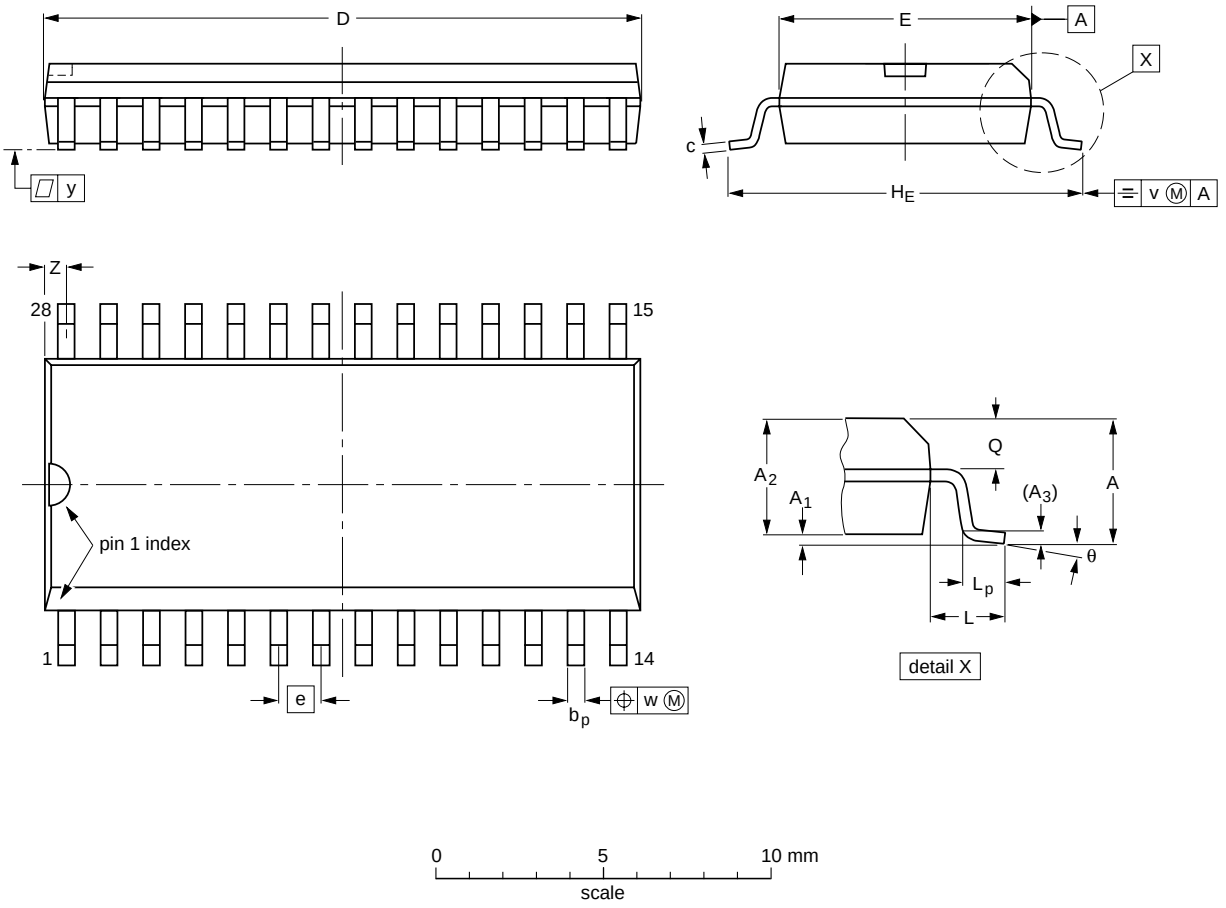
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.1	0.51	4.0	1.7 1.3	0.53 0.38	0.32 0.23	36.0 35.0	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	1.7
inches	0.20	0.020	0.16	0.066 0.051	0.020 0.014	0.013 0.009	1.41 1.34	0.56 0.54	0.10	0.60	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.067

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT117-1	051G05	MO-015AH				~~92-11-17~~ 95-01-14

SO28: plastic small outline package; 28 leads; body width 7.5 mm **SOT136-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	18.1 17.7	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.71 0.69	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT136-1	075E06	MS-013AE				~~95-01-24~~ 97-05-22

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

DIP

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

SO

Reflow soldering

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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